

## **What is claimed is:**

**[Claim 1]** 1. A dynamic random access memory (DRAM) cell, comprising:  
a semiconductor pillar on a substrate;  
a capacitor on a lower portion of a sidewall of the pillar, comprising:  
a first plate in the lower portion of the sidewall of the pillar;  
a second plate as an upper electrode at periphery of the first plate;  
a third plate at periphery of the second plate, electrically connecting with the first plate to form a lower electrode together; and  
a dielectric layer, separating the second plate from the first plate and the third plate; and  
a vertical transistor on an upper portion of the sidewall of the pillar, electrically coupled with the capacitor.

**[Claim 2]** 2. The DRAM cell of claim 1, wherein  
the first plate and the third plate are electrically connected via a design wherein the first plate further extends to the substrate beside the pillar and the third plate contacts with the substrate beside the pillar; and  
the dielectric layer is also disposed on a portion of the first plate in the substrate beside the pillar to separate a bottom of the second plate from the first plate.

**[Claim 3]** 3. The DRAM cell of claim 2, wherein the dielectric layer comprises:  
a first dielectric layer between the pillar and the second plate and between the substrate and the second plate; and  
a second dielectric layer between the second plate and the third plate, connecting with the first dielectric layer.

**[Claim 4]** 4. The DRAM cell of claim 1, wherein the second plate has a top portion directly contacting with a source/drain region of the vertical transistor in the pillar.

**[Claim 5]** 5. The DRAM cell of claim 1, wherein the first plate, the second plate, the third plate and the dielectric layer surround the pillar.

**[Claim 6]** 6. The DRAM cell of claim 5, wherein the capacitor further comprises:

a collar insulating layer surrounding the pillar and covered by an upper portion of the second plate.

**[Claim 7]** 7. The DRAM cell of claim 6, wherein the second plate comprises:

a first conductor surrounding the collar insulating layer;  
a second conductor under the first conductor and the collar insulating layer;  
and  
a third conductor on the first conductor and the collar insulating layer, electrically coupled with the vertical transistor.

**[Claim 8]** 8. The DRAM cell of claim 1, wherein the vertical transistor comprises,

a first doped region in the sidewall of the pillar, electrically connected with the upper electrode of the capacitor;  
a second doped region in a top portion of the pillar;  
a gate on the sidewall of the pillar between the first doped region and the second doped region; and  
a gate insulating layer between the sidewall of the pillar and the gate.

**[Claim 9]** 9. The DRAM cell of claim 8, wherein the gate is separated from a top portion of the upper electrode by an insulator.

**[Claim 10]** 10. The DRAM cell of claim 8, wherein the first doped region, the gate and the gate insulating layer surround the pillar.

**[Claim 11]** 11. A dynamic random access memory (DRAM) array, comprising:

rows and columns of memory cells disposed on a substrate, each comprising:  
a semiconductor pillar on the substrate;  
a capacitor on a lower portion of a sidewall of the pillar, comprising a first plate in the lower portion of the sidewall of the pillar, a second plate as an upper electrode at periphery of the first plate, a third plate disposed at

periphery of the second plate and electrically connected with the first plate to form a lower electrode together, and a dielectric layer separating the second plate from the first plate and the third plate; and  
a vertical transistor on an upper portion of the sidewall of the pillar, electrically coupled with the capacitor;  
a plurality of bit lines, each coupled with one row of vertical transistors; and  
a plurality of word lines, each coupled with one column of vertical transistors.

**[Claim 12]** 12. The DRAM array of claim 11, wherein  
the first plates are electrically connected with each other via a doped surface layer of the substrate between the pillars;  
the third plates together constitute a conductive layer partially filling the space between the pillars and contacting with the doped surface layer of the substrate; and  
the first plates, the doped surface layer and the conductive layer together serve as a common lower electrode.

**[Claim 13]** 13. The DRAM array of claim 12, wherein in each memory cell, the dielectric layer comprises:  
a first dielectric layer between the second plate and the pillar and between the second plate and the doped surface layer of the substrate; and  
a second dielectric layer between the second plate and the third plate, connecting with the first dielectric layer.

**[Claim 14]** 14. The DRAM array of claim 11, wherein each second plate has a top portion directly contacting with a source/drain region of a corresponding vertical transistor.

**[Claim 15]** 15. The DRAM array of claim 11, wherein in each capacitor, the first plate, the second plate, the dielectric layer and the third plate surround the pillar.

**[Claim 16]** 16. The DRAM array of claim 15, wherein each capacitor further comprises a collar insulating layer that surrounds the corresponding pillar and is covered by an upper portion of the second plate.

**[Claim 17]** 17. The DRAM array of claim 16, wherein the second plate comprises:

a first conductor surrounding the collar insulating layer;  
a second conductor under the first conductor and the collar insulating layer;  
and  
a third conductor on the first conductor and the collar insulating layer,  
electrically coupled with a corresponding vertical transistor.

**[Claim 18]** 18. The DRAM array of claim 11, wherein each vertical transistor comprises:

a first doped region in the sidewall of a corresponding pillar, electrically connected with the upper electrode of a corresponding capacitor;  
a second doped region in a top portion of the pillar;  
a gate on the sidewall of the pillar between the first doped region and the second doped region; and  
a gate insulating layer between the sidewall of the pillar and the gate.

**[Claim 19]** 19. The DRAM array of claim 18, wherein each bit line directly contacts with the second doped regions of the vertical transistors of the memory cells in one row.

**[Claim 20]** 20. The DRAM array of claim 18, wherein the gates of the memory cells in one column are connected to each other to form a gate line.

**[Claim 21]** 21. The DRAM array of claim 20, wherein the gate line directly serves as a word line for the vertical transistors in the column.

**[Claim 22]** 22. The DRAM array of claim 20, wherein a word line is electrically connected to the gate line via at least one contact between two pillars.

**[Claim 23]** 23. A method for fabricating a DRAM array, comprising:  
patterning a semiconductor substrate to form rows and columns of pillars thereon;

forming a capacitor on a lower portion of a sidewall of each pillar, comprising:  
forming a first plate in the lower portion of the sidewall of each pillar;  
forming a first dielectric layer at periphery of each first plate;  
forming a second plate as an upper electrode at periphery of each first dielectric layer;  
forming a second dielectric layer at periphery of each second plate; and  
forming a third plate at periphery of each second dielectric layer, wherein the third plate is electrically connected with a corresponding first plate to form an lower electrode;  
forming a vertical transistor on an upper portion of a sidewall of each pillar, the vertical transistor being coupled with a corresponding capacitor; and  
forming a plurality of bit lines over the substrate, wherein each bit line is coupled with one row of vertical transistors.

[Claim 24] 24. The method of claim 23, wherein the first plates are formed together with a doped surface layer of the substrate between the pillars, so that all first plates are electrically connected with each other.

[Claim 25] 25. The method of claim 24, wherein the step of forming the first dielectric layer comprises forming a conformal dielectric layer on the doped surface layer of the substrate and the sidewall of each pillar.

[Claim 26] 26. The method of claim 25, wherein the step of forming the third plates comprises:

removing the first dielectric layer exposed by the second plate and the second dielectric layer to expose a portion of the doped surface layer between the pillars; and  
forming a conductive layer partially filling the space between the pillars to serve as the third plates of all capacitors.

[Claim 27] 27. The method of claim 25, wherein the step of forming the second plate comprises:

forming at least one conductive layer partially filling the space between the pillars;  
forming a spacer on the sidewall of each pillar; and  
using the spacers as a mask to etch the conductive layer into the second plates.

[Claim 28] 28. The method of claim 27, wherein the steps of forming the second dielectric layers and the third plates comprise:

forming a dielectric spacer on sidewalls of each spacer and the corresponding second plate, wherein a lower portion of each dielectric spacer serves as the second dielectric layer;  
using the spacers and the dielectric spacers as an etching mask to remove the exposed first dielectric layer;  
forming a second conductive layer partially filling the space between to serve as the third plates of all capacitors; and  
removing each spacer and an upper portion of each dielectric spacer.

[Claim 29] 29. The method of claim 27, wherein the step of forming the at least one conductive layer comprises:

forming a first conductive layer partially filling the space between the pillars;  
removing portions of the conformal dielectric layer exposed by the first conductive layer;  
forming an insulating spacer on the sidewall of each pillar above the first conductive layer;  
forming a second conductive layer between the pillars to cover lower portions of the insulating spacers;  
removing a portion of each insulating spacer exposed by the second conductive layer to form a collar insulating layer on each pillar; and  
forming a third conductive layer between the pillars and on the collar insulating layers and the second conductive layer.

[Claim 30] 30. The method of claim 23, wherein in each memory cell, a top portion of the second plate directly contacts with the pillar.

**[Claim 31]** 31. The method of claim 23, wherein the step of forming the vertical transistors comprises:

partially filling the space between the pillars with a first insulating material to cover the capacitors;  
forming a gate structure of a vertical transistor on the sidewall of each pillar above the first insulating layer, the gate structure comprising a gate electrode and a gate insulating layer between the pillar and the gate electrode;  
forming a first doped region of a vertical transistor in the sidewall of each pillar coupling with the capacitor on the sidewall of the same pillar; and  
forming a second doped region of a transistor in a top portion of each pillar.

**[Claim 32]** 32. The method of claim 31, wherein the step of forming the gate structure comprises:

forming a gate insulating layer on the sidewall of each pillar above the first insulating material;  
forming a conductive layer between the pillars and on the first insulating material, the conductive layer having a top surface lower than the top surface of the pillar;  
forming a mask spacer on the sidewall of each pillar above the conductive layer;  
forming a mask layer comprising a plurality of linear patterns over the substrate, wherein each linear pattern runs over the pillars in one column; and  
etching the conductive layer using the mask spacer and the mask layer as a mask to form a gate on the sidewall of each pillar, wherein the gates on the pillars in one column are connected via the conductive layer between the pillars of the same column to form a gate line.

**[Claim 33]** 33. The method of claim 32, further comprising forming a plurality of word lines over the substrate after the bit lines are formed, wherein each word line is formed crossing over the bit lines to electrically connect a corresponding gate line via at least one contact between the pillars of the corresponding column.

**[Claim 34]** 34. The method of claim 33, wherein the step of forming the word lines comprises:

forming a dielectric layer over the substrate covering the bit lines; and forming at least one contact through the dielectric layer and a word line on the dielectric layer to electrically connect with the gate line, wherein the contact directly contacts the conductive layer between two pillars of the same column.

[Claim 35] 35. The method of claim 34, wherein each bit line is formed with a cap layer thereon; and the method further comprises: forming a protective spacer on sidewalls of each pair of bit line and cap layer before the dielectric layer is formed.

[Claim 36] 36. The method of claim 34, wherein the contact and the word line are formed with a damascene process.

[Claim 37] 37. The method of claim 31, wherein in each memory cell, the first doped region in the sidewall of the pillar is formed through dopant diffusion from a top portion of the second plate, wherein the top portion of the second plate directly contacts with the pillar.

[Claim 38] 38. The method of claim 31, wherein each bit line is formed directly contacting with the second doped regions of the transistors in one row.

[Claim 39] 39. The method of claim 38, wherein before each bit line is formed, the space between the pillars is filled with a second insulating material covering the transistors.

[Claim 40] 40. The method of claim 23, further comprising forming a plurality of word lines over the substrate after the bit lines are formed, wherein each word line is coupled with one column of vertical transistors.